THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No	10/624,627
	July 21, 2003
	Luan C. Tran
Assignee	Micron Technology, Inc.
	2812
Examiner	Kennedy, Jennifer M.
Attorney's Docket No	Ml22-2358
Title:	Methods of Forming Semiconductor Constructions

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR § 1.56. Copies of the cited art are included with the exception of U.S. patents and published U.S. applications (1276 OG 55). No admission is made regarding whether all the submitted references are prior art.

Respectfully submitted,

Dated:

Ву:

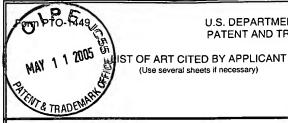
Jennifer J./Taylor, Ph

Reg. No. 48,711

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ATTY. DOCKET NO. MI22-2358

SERIAL NO. 10/624,627

APPLICANT: Luan C. Tran

FILING DATE **GROUP** July 21, 2003 2812 U.S. PATENT DOCUMENTS Class Subclass Filing Date Date Name *Examiner's Document Initials Number If Appropriate AA 5,534,456 07/96 Yuan et al. 5,970,352 10/99 Shiozawa et al. AC 6,001,707 12/99 Lin et al. ΑĐ 6,420,749 07/02 Divakaruni et al. ΑE 6,187,624 02/01 Huang AF 5,946,568 08/99 Hsiao et al. AG 06/01 6,242,329 Huster et al. AΗ 05/99 Shin 5,904,530 US2002/0006693 01/02 Matsuda FOREIGN PATENT DOCUMENTS Class Translation Document Date Country SubclasS Number No ΑJ 04/92 JP04105328A Japan ΑK AL OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.) Wolf et al., Silicon Processing for the VLSI Era, Vol. 1: "Process Technology," Second Edition, Lattice Press 2000, pp. 12-13, 25-27. S.M. Sze, VLSI Technology, Second Edition, McGraw-Hill, 1988, pages 472-483 AO **EXAMINER** DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.